IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application:	:	Group Art Unit: 1733
S. Kobayashi	:	Examiner: J. T. Haran
Serial No.: 10/068,400	:	IBM Corporation
Filed: 02/06/2002	:	Intellectual Property Law
Title: BONDING METHOD AND APPARATUS	:	Department IQ0A/040-3
	:	1701 North Street
	:	Endicott, NY 13760

Assistant Commissioner For Patents

Washington, DC 20231

Sir:

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Assistant Commissioner For Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on 1/20/05

Georgia Brundege 1/20/05

Georgia Y. Brundege Date

REQUEST FOR REINSTATEMENT OF APPEAL

Appellants filed a Notice of Appeal on Jun 29, 2004 and an Appeal Brief on August 30, 2004 due to a first Final Rejection on April 2, 2004. The Examiner mailed a second Final Rejection on September 23, 2004, after Appellants mailed their Appeal Brief. Under Rule 1.193 (b) (2) (ii), Appellants request reinstatement of the Appeal. A Supplemental Appeal Brief is included to address a new ground of rejection raised by the Examiner in the second Final Rejection of September 23, 2004.

The Commissioner is authorized to charge any additional fees associated with this Request for Reinstatement of Appeal to Deposit Account number 09-0457.

Respectfully submitted,

Arthur Samodovitz
Reg. No. 31,297

Docket No: JP920000346US1
Phone: (607) 429-4368
Fax: (607) 429-4119

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SUPPLEMENTAL APPEAL BRIEF

I. Real Party in Interest

The real party in interest is International Business Machines Corporation.

II. Related Appeals and Interferences

There are no related appeals or interferences.

III. Status of Claims

Claims 1-21 were previously canceled.

Claims 22-41 are pending.

Claims 25, 32 and 39 are appealed.

IV. Status of Amendments

An amendment after Final Action was filed on June 28, 2004 (and received on July 2, 2004), but this Amendment was not entered.

V. Summary of the Invention

Dependent claim 25 (including base claim 22) recites a method of forming a bonded assembly. An IC chip (21) is positioned adjacent to a substrate (23) with a thermosetting adhesive (24) between the IC chip and the substrate to adhere the IC chip to the substrate. The substrate comprises an epoxy resin reinforced with fiberglass. See Figure 1 and page 8 lines 9-11. The substrate is irradiated with near infrared light toward the IC chip such that some energy of the light is absorbed by the substrate and some energy of the light passes through the substrate to the adhesive to partially cure the adhesive. See page 14 lines 12-25. Claim 25 also recites the step of halting the irradiating step after the adhesive is heated to a predetermined, curing temperature, and after the halting step, cooling the assembly to substantially room temperature and **applying pressure on the IC chip toward the substrate during substantially the entirety of the cooling step**. There is support for this latter part of claim 25 as follows:

"a heating/pressuring system 10 for heating and pressurizing silicon chip 21 ... Heating/pressurizing system 10 comprises a pressurizing block 11, heat insulator 12, heater tool 13, pressure buffer 14, holding (or supporting) block 15 (preferably made of fused silica for industrial use), and back-up blocks 16." Page 8 lines 17-23. "Next, description will be made regarding a cooling system for cooling down the heat generated by the assembly apparatus of the embodiment. The cooling system preferably comprises three cooling nozzles 41a, 41b and 41c, a heat sink 42 and cooling fins 43. At least one of the cooling nozzles (i.e., 41a in FIG. 1) is provided to prevent excessive heat generated by heater tool 13 from reaching polarizer 26 via the pressure buffer 14." Page 11 lines 5-10. "Heater tool 13 is cooled by supplying a cooling medium to cooling hole 44a. Similarly, supporting block 15 is cooled by supplying a cooling medium to cooling holes 44b and 44c." Page 11 line 24 to Page 12 line 2. "Since the thermal conductive heating by heater tool 13 is performed during application of pressure by block 11 onto pressure buffer 14, pressure buffer 14 is also heated." Page 13 lines 9-10.

"When thermosetting ACF 24 is heated up to a specified temperature, irradiation of near infrared rays 36 is terminated. In the next step, silicon chip 21 and array substrate 23 are pressed together by pressure indirectly applied to silicon chip 21 by pressurizing block 11 (S 105). As understood, substrate 23 is firmly supported by block 15. Thereafter, silicon chip 21, thermosetting ACF 24 and array substrate 23 are cooled to room temperature (S 106). Here, silicon chip 21 and the glass component that constitute array substrate 23 have approximately the same degrees of contraction. Thus, in this cooling process, an unacceptable temperature difference (gradient) between the silicon chip and array substrate is prevented in order to achieve such uniform contraction." Page 14 line 24 to page 15 line 6.

"The preferred method of cooling the above-heated structure will now be described with reference to FIGS. 5A to 5C." Page 17 lines 16-17. "As taught herein, heating of silicon chip 21 by heater tool 13 at this time prevents silicon chip 21 from cooling down too rapidly. Such heating is referred to as subheating (following the full heating procedure defined above). In comparison, array substrate 23 is relatively slow in cooling down compared to the chip. Cooling of array substrate 23 is accelerated by utilizing air flow through cooling holes 44b and 44d, thus reducing the temperature difference between the substrate and silicon chip 21 to an acceptable level. Cooling of silicon chip 21, thermosetting ACF 24 and array substrate 23 progresses as shown in FIG. 5B, while performing subheating of the chip and accelerated cooling of the substrate as described above. Continued "cooling down", including the defined subheating and acceleration of cooling silicon chip 21, thermosetting ACF 24 and array substrate 23 are cooled down to room temperature, this as shown in FIG. 5C. In this way, the invention avoids the occurrence of cambers because of the treatment for suppressing the temperature difference between silicon chip 21 and array substrate during the cooling process, which preferably allows such temperature differences to reach virtually zero." Page 18 lines 9-23.

VI. Issues

Claims 25, 32 and 39 were newly rejected under 35 USC 112, first paragraph. Therefore, the new issue is whether there is sufficient support in the specification for these claims. (This

issue was first raised in the second Final Office Action mailed 9/24/2004, after filing of Applicants' Appeal Brief.)

Claims 25, 32 and 39 were rejected under 35 USC 103(a) in view of Oxman et al in view of Uchiyama et al. (US Patent 5, 847,796). Therefore another issue is whether these claims were obvious in view of Oxman et al. and Uchiyama et al. (This issue was raised before the Notice of Appeal was filed.)

Claims 25, 32 and 39 were rejected under 35 USC 103(a) in view of Uchiyama et al, the admitted prior art and Oxman et al. Therefore another issue is whether these claims were obvious in view of Oxman et al., Uchiyama et al. and admitted prior art. (This issue was raised before the Notice of Appeal was filed.)

Claim 39 was also objected to under 37 CFR 1.75 as being a substantial duplicate of claim 25. Therefore another issue is whether these two claims are so close as to prevent allowance of both. (This issue was raised before the Notice of Appeal was filed.)

VII. Grouping of Claims

Group I: 25 and 39

Group II: 32

The claims do not all stand or fall together. Rather each group of claims has independent grounds of patentability.

VIII. Argument

Rejection under 35 USC 112, first paragraph

Claims 25, 32 and 39 were rejected under 35 USC 112, first paragraph. Appellants respectfully traverse this rejection based on the following.

Claim 25 recites the step of halting the irradiating step after the adhesive is heated to a predetermined, curing temperature, and after the halting step, cooling the assembly to substantially room temperature and **applying pressure on the IC chip toward the substrate during substantially the entirety of the cooling step**. The support for claim 25 is excerpted above. As noted above, "heating/pressurizing system 10 comprises a pressurizing block 11, heat insulator 12, heater tool 13, pressure buffer 14, holding (or supporting) block 15 (preferably made of fuses silica for industrial use), and back-up blocks 16." Page 8 lines 17-23. As illustrated in Figure 1, the pressuring block 11 applies its pressure by gravity, as it rests on the pressure buffer 14. Pressure buffer 14 rests on chip 21. Chip 21 rests on substrate 23 (with intervening adhesive 24), and substrate 23 rests on support block 15. The adhesive 24 bonds the chip to the substrate 23. During the initial process of curing adhesive 24, the heater unit preheats chip 21, and then the infrared heating unit 31 heats the substrate. Afterwards, the cooling process begins. To prevent the chip 21 from cooling faster than substrate 23 due to the lower mass of chip 21 (and causing temperature differentials and warping), the chip 21 is heated to some degree during the cooling process.

> "**As taught herein, heating of silicon chip 21 by heater tool 13 at this time prevents silicon chip 21 from cooling down too rapidly**. Such heating is referred to as subheating (following the full heating procedure defined above). In comparison, array substrate 23 is relatively slow in cooling down compared to the chip. Cooling of array substrate 23 is accelerated by utilizing air flow through cooling holes 44b and 44d, thus reducing the temperature difference between the substrate and silicon chip 21 to an acceptable level. Cooling of silicon chip 21, thermosetting ACF 24 and array substrate 23 progresses as shown in FIG. 5B, while performing subheating of the chip and accelerated cooling of the substrate as described above. **Continued "cooling down", including the defined subheating and acceleration of cooling silicon chip 21, thermosetting ACF 24 and array substrate 23 are cooled down to room temperature, this as shown in FIG. 5C.** In this way, the invention avoids the occurrence of cambers because of the treatment for suppressing the temperature

difference between silicon chip 21 and array substrate during the cooling process, which preferably allows such temperature differences to reach virtually zero." Page 18 lines 9-23.

The cooling process is also described as follows:

"When thermosetting ACF 24 is heated up to a specified temperature, irradiation of near infrared rays 36 is terminated. **In the next step, silicon chip 21 and array substrate 23 are pressed together by pressure indirectly applied to silicon chip 21 by pressurizing block 11 (S 105). As understood, substrate 23 is firmly supported by block 15. Thereafter, silicon chip 21, thermosetting ACF 24 and array substrate 23 are cooled to room temperature (S 106).** Here, silicon chip 21 and the glass component that constitute array substrate 23 have approximately the same degrees of contraction. Thus, in this cooling process, an unacceptable temperature difference (gradient) between the silicon chip and array substrate is prevented in order to achieve such uniform contraction." Page 14 line 24 to page 15 line 6.

Thus, in step 105, pressure is applied. During the cooling process in step 106, there is still some heating of the chip 21 by the heater 13, as explained above. **There is no mention in step 106 or in the description of FIG. 5C that the pressure block 11 is removed during the cooling process and because heating by heater 13 continues during the cooling process, it follows that pressure block 11, which is part of the heating/pressurizing system 10, remains on the heater 13 during cooling of the chip to room temperature.** Therefore, there is support in the specification for claim 25, as well as claims 32 and 39, and the rejection under 35 USC 112, first paragraph should be withdrawn.

Rejection under 35 USC 103

Claims 25, 32 and 39 were rejected under 35 USC §103 based on Oxman et al. in view of Uchiyama et al and in view of admitted prior art.

Appellants respectfully traverse this rejection based on the following.

Group I

Dependent claim 25 (including base claim 22) recites a method of forming a bonded assembly. An IC chip is positioned adjacent to a substrate with a thermosetting adhesive between the IC chip and the substrate to adhere the IC chip to the substrate. The substrate comprises an epoxy resin reinforced with fiberglass. The substrate is irradiated with near infrared light toward the IC chip such that some energy of the light is absorbed by the substrate and some energy of the light passes through the substrate to the adhesive to partially cure the adhesive. Claim 25 also recites the step of halting the irradiating step after the adhesive is heated to a predetermined, curing temperature, and after the halting step, cooling the assembly to substantially room temperature and **applying pressure on the IC chip toward the substrate during substantially the entirety of the cooling step**. This is described in the specification of the present invention,

> "When thermosetting ACF 24 is heated up to a specified temperature, irradiation of near infrared rays 36 is terminated. In the next step, silicon chip 21 and array substrate 23 are pressed together by pressure indirectly applied to silicon chip 21 by pressurizing block 11 (S 105). As understood, substrate 23 is firmly supported by block 15. Thereafter, silicon chip 21, thermosetting ACF 24 and array substrate 23 are cooled to room temperature (S 106). Here, silicon chip 21 and the glass component that constitute array substrate 23 have approximately the same degrees of contraction. Thus, in this cooling process, an unacceptable temperature difference (gradient) between the silicon chip and array substrate is prevented in order to achieve such uniform contraction." Page 14 line 24 to page 15 line 6.

The Examiner notes that Oxman et al. is silent as to this last feature. "Regarding claims 25, 32 and 39, Oxman et al. is silent towards applying pressure to the chip after the adhesive has been heated to a curing temperature and the irradiation stopped until the assembly has cooled to room

temperature." The Examiner also notes that Uchiyama et al. does not teach this feature either. "It is noted that Uchiyama does not teach applying pressure until the assembly has cured to room temperature" but asserts that "one skilled in the art would have readily appreciated that when the pressure is stopped is a function of a variety of factors and would have appreciated maintaining pressure until the assembly reached room temperature to ensure adequate adhesion and to prevent warpage while cooling." There is no documentary basis for the Examiner's assertion.

Uchiyama et al. teach the removal of the pressure during cooling below 150 degrees C:

> "The bonding conditions include a temperature 220 degrees C, a pressure of 5 gf/mm squared, and a time of 20 seconds. The quality of the light applied and the pressure are set so as to establish these conditions. Then, heating by the light 13 is stopped to decrease the temperature to 150 degrees C under pressure by the bonding tool 4 and **pressing by the bonding tool 4 is then stopped."** (Emphasis added) Column 14 lines 20-27

Thus, Uchiyama et al. teach that the pressure is maintained only until the temperature drops to 150 degrees C, not during subsequent cooling. In contrast, claim 25 recites that the pressure is applied until the assembly is cooled to substantially room temperature. Therefore, Uchiyama et al. teach away from the present invention, and claim 25 would not have been obvious in view of Uchiyama et al. The admitted prior art of FR-4 as a conventional dielectric material for a substrate or even an LCD does not close the gap. Therefore, the rejection of claim 25 should be reversed.

Claim 39 similarly distinguishes over Oxman et al., Uchiyama et al. and admitted prior art.

Group II

Claim 32 is similar to claim 25 except claims 32 states that "said light passes through said substrate to said adhesive to at least partially cure said adhesive" whereas claim 25 recites "said

light passes through said substrate to said adhesive to substantially cure said adhesive". Therefore, claim 32 distinguishes over Oxman et al., Uchiyama et al. and admitted prior art for the same reasons as does claim 25, and the rejection under 35 USC § 103 should be reversed.

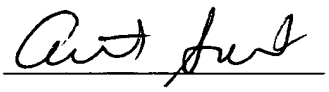
Rejection under 37 CFR 1.75

Claims 39 was also objected to under 37 CFR 1.75 as being a substantial duplicate of claims 25. Appellants respectfully traverse this objection based on the following.

Claim 25 recites in part, "irradiating said substrate with near infrared light toward said IC chip such that **some energy of said light** is absorbed by said substrate and **some energy of said light** passes through said substrate to said adhesive to substantially cure said adhesive". Claim 39 recites in part, "irradiating said substrate with near infrared light toward said IC chip such that **some of said light** is absorbed by said substrate and **some of said light** passes through said substrate to said adhesive to substantially cure said adhesive".

Based on the foregoing, Appellants request that the rejections of claims 25, 32 and 39 under 35 USC 112, first paragraph and under 35 USC 103 be reversed, and the objection of claim 39 under 37 CFR 1.75 be reversed.

Respectfully submitted,



Arthur Samodovitz

Reg. No. 31,297

IX. Appendix: Only claims involved in the Appeal

22. A method of forming a bonded assembly, said method comprising the steps of:

positioning an IC chip adjacent to a substrate with a thermosetting adhesive between said IC chip and said substrate to adhere said IC chip to said substrate, said substrate comprising an epoxy resin reinforced with fiberglass; and

irradiating said substrate with near infrared light toward said IC chip such that some energy of said light is absorbed by said substrate and some energy of said light passes through said substrate to said adhesive to substantially cure said adhesive.

25. A method as set forth in claim 22 further comprising the step of halting the irradiating step after said adhesive is heated to a predetermined, curing temperature, and after the halting step, cooling said assembly to substantially room temperature and applying pressure on said IC chip toward said substrate during substantially the entirety of said cooling step.

29. A method of forming a bonded assembly, said method comprising the steps of:

positioning an IC chip adjacent to a substrate with a thermosetting adhesive between said IC chip and said substrate to adhere said IC chip to said substrate, said substrate comprising an epoxy resin reinforced with fiberglass; and

irradiating said substrate with near infrared light toward said IC chip such that some energy of said light is absorbed by said substrate and some energy of said light passes through said substrate to said adhesive to at least partially cure said adhesive.

32. A method as set forth in claim 29 further comprising the step of halting the irradiating step after said adhesive is heated to a predetermined, curing temperature, and after the halting step, cooling said assembly to substantially room temperature and applying pressure on said IC chip toward said substrate during substantially the entirety of said cooling step.

36. A method of forming a bonded assembly, said method comprising the steps of:

positioning an IC chip adjacent to a substrate with a thermosetting adhesive between said IC chip and said substrate to adhere said IC chip to said substrate, said substrate comprising an epoxy resin reinforced with fiberglass; and

irradiating said substrate with near infrared light toward said IC chip such that some of said light is absorbed by said substrate and some of said light passes through said substrate to said adhesive to substantially cure said adhesive.

39. A method as set forth in claim 36 further comprising the step of halting the irradiating step after said adhesive is heated to a predetermined, curing temperature, and after the halting step, cooling said assembly to substantially room temperature and applying pressure on said IC chip toward said substrate during substantially the entirety of said cooling step.